REMARKS

Applicants hereby add claims 23-28 and claims 1-28 are pending in the present application. Claims 1, 3-13, 15-17 and 19-22 stand rejected for anticipation by U.S. Patent No. 4,256,977 to Hendrickson. Claims 2, 14 and 18 stand rejected for obviousness over Hendrickson.

Applicants respectfully traverse the rejections and urge allowance of the present application.

On page 2 of the Action, it is stated that Hendrickson discloses a power semiconductor switching device comprising field effect transistors 41, 42. Auxiliary circuitry 43 is identified as allegedly disclosing the claimed auxiliary circuitry.

Applicants have amended claim 1 to clarify limitations inherent in originally-filed claim 1. For example, claim 1 now recites a plurality of field effect transistors *coupled in parallel with one another to form a power semiconductor switching device and wherein respective ones of the power contacts of the field effect transistors are coupled in common with one another.* Hendrickson fails to disclose or suggest the integrated circuitry defined by claim 1. Transistors 41, 42 of Hendrickson and identified in the Office Action as allegedly disclosing the claimed plural field effect transistors are not coupled in parallel and the power connections thereof are not coupled in common with one another. Capacitor 30 of Fig. 6. is provided intermediate contacts of transistors 41, 42. Accordingly, Hendrickson fails to disclose or suggest limitations of claim 1 and claim 1 is allowable.

In addition, the field effect transistors 41, 42 of Hendrickson are in no fair interpretation arranged to form a *power* semiconductor switching device as recited in claim

1. Referring to the teachings in column 8, lines 58-65 of Hendrickson, it is stated that Fig. 6 is equivalent to the circuit of Fig. 3 but having an electronic implementation for switch 32 of Fig. 3. As shown in Fig. 6, transistors 41, 42 are arranged to form switch means 32 as set forth in column 9, lines 3-5 of Hendrickson. Transistors 41, 42 arranged to implement switching functionality of switch means 32 in no fair interpretation disclose or suggest field effect transistors coupled in parallel with one another to form a power semiconductor switching device as recited in claim 1. Claim 1 recites limitations not shown or suggested in the prior art of record and claim 1 is allowable for at least this reason.

The claims which depend from independent claim 1 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

For example, claim 2 stands rejected for obviousness as set forth on page 3 of the Action. The Office Action states that Hendrickson does not disclose planar field effect transistors but states that it would have been within the level of ordinary skill in the art to use planar field effect transistors. Applicants disagree with the obviousness rejection of claim 2 for the below numerous reasons.

Claim 1 recites the field effect transistors are coupled in parallel to form a *power semiconductor switching device* and claim 2 specifies that the field effect transistors which form the power semiconductor switching device comprise planar field effect transistors. The prior art is entirely devoid of disclosing or suggesting planar field effect transistors coupled in parallel with one another to form a power semiconductor switching device. Applicants respectfully traverse the statement that it would have been within the level of

ordinary skill in the art to use planar field effect transistors. The record is entirely devoid of any support for the bald, cursory statement set forth in section 4 on page 3 of the Action stating that limitations of claim 2 would have been within the level of ordinary skill. In conjunction with such traversal and pursuant to MPEP 2144.03, Applicants respectfully request the submission in a *non-final action* of an affidavit from the Examiner or prior art reference in support of any rejection of claim 2 if claim 2 is not found to be allowable.

Referring now to MPEP §2143.01 (8th ed.), there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify or combine reference teachings. The mere fact that references *can* be combined or modified does not render the resultant combination obvious *unless the prior art also suggests the desirability of the combination*. MPEP §2143.01 *citing In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Obviousness cannot be established by a combination of references unless there is some motivation in the art to support the combination. *See ACH Hospital Systems, Inc. v. Montifiore Hospital*, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). The motivation for forming the combination must be something other than hindsight reconstruction based on using Applicant's invention as a road map for such a combination. *See, e.g., Interconnect Planning Corp. v. Feil*, 227 USPQ 543, 551 (Fed. Cir. 1985); *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990).

There is absolutely no motivation for one of skill in the art to modify the teachings of Hendrickson. Transistors 41, 42 of Hendrickson clearly relate to switching devices to provide switching functionality of switch means 32. Devices 41, 42 provide no teachings

or suggestion of planar field effect transistors coupled in parallel to form a power semiconductor switching device. Such modification of Hendrickson teachings is contrary to the switching operations implemented by transistors 41, 42 of switch means 32. There is no motivation to modify the Hendrickson teachings to arrive at the limitations of claim 2 and claim 2 is allowable for at least this additional reason.

Referring to the anticipation rejection of claim 3, on page 2 of the Office Action it is stated that reference 43 comprises a gate driver amplifier configured to provide a control signal to the electrical contacts of the field effect transistors comprising the gate contacts. Applicants have electronically searched the Hendrickson patent and have failed to uncover any gate driver amplifier teachings. The Office Action fails to identify specific reference teachings relied upon as allegedly anticipating the limitations of claim 3. Further, the switch control circuitry 43 of Hendrickson provides plural control signals to transistors 41, 42. Hendrickson fails to disclose or suggest the claimed gate driver amplifier configured to provide *a control signal* to the electrical contacts of the field effect transistors comprising the gate contacts. Claim 3 is allowable over the prior art of record.

Referring to claim 6, it is stated on page 2 of the Action that claim 6 is anticipated by Hendrickson without identification of any teachings which allegedly disclose the claimed application specific integrated circuit limitation. Applicants have electronically searched Hendrickson and have failed to uncover any ASIC or application specific integrated circuit teachings. Hendrickson fails to disclose or suggest positively recited limitations of claim 6 and claim 6 is allowable for at least this reason.

Referring to claim 7, the Office Action fails to identify any teachings which allegedly

disclose the claimed zero-current switching/timing circuit limitation. Applicants have electronically searched and have failed to uncover any zero-current switching/timing circuit teachings in Hendrickson. Positively recited limitations of claim 7 are not shown or suggested in the art and claim 7 is allowable for at least this reason.

Referring to claim 12, it is stated in section 2 on page 2 of the Action that claim 12 is anticipated by Hendrickson. Thereafter, a recitation of alleged Hendrickson teachings proceeds with respect to limitations of claim 1 but is entirely devoid of identifying any teachings of Hendrickson which allegedly correspond to limitations of claim 12. Hendrickson fails to disclose or suggest forming a *power field effect transistor* using a monolithic substrate and *having a source contact and a drain contact adjacent to the surface of the monolithic semiconductor substrate* as recited in claim 12. Accordingly, Hendricksen fails to disclose or suggest positively-recited limitations and claim 12 is allowable for at least this reason.

Further, Hendrickson fails to disclose or suggest coupling the auxiliary circuitry with at least one contact of the power field effect transistor. The transistors identified in the Office Action of references 41, 42 of Hendrickson are switching transistors and fail to disclose or suggest limitations of claim 12 defining forming a power field effect transistor. Numerous limitations of claim 12 are not shown or suggested in the prior art of record and claim 12 is allowable for at least this reason.

The claims which depend from independent claim 12 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

For example, claim 14 recites forming the power field effect transistor comprising forming a plurality of *planar field effect transistors electrically coupled in parallel*. References 41, 42 of Hendrickson fail to disclose or suggest limitations of claim 14 and claim 14 is allowable for at least this reason.

Applicants submit herewith a Form PTO-1449 which has not been initialed by the Examiner, request initialization of the form, and forwarding of the initialed form to Applicants.

Applicants submit a supplemental Information Disclosure Statement herewith.

Applicant respectfully requests allowance of all pending claims.

The Examiner is requested to phone the undersigned if the Examiner believes such would facilitate prosecution of the present application. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: 8/12/02

By: _____

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Inventor ..... Richard C. Eden et al.
Assignee ..... Isothermal Systems Research, Inc.
Group Art Unit 2812
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Title: Power Semiconductor Switching Devices, Power Converters, Integrated Circuit Assemblies, Integrated Circuitry, Power Current Switching Methods, Methods of Forming a Power Semiconductor Switching Device, Power Conversion Methods, Power Semiconductor Switching Device Packaging Methods, and Methods of Forming a Power Transistor

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO APRIL 11, 2002 OFFICE ACTION

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

1. (Amended) Integrated circuitry comprising:

a monolithic semiconductive substrate;

~~a power semiconductor switching device comprising a plurality of field effect transistors formed using the monolithic semiconductive substrate and having a plurality of electrical contacts including a plurality of gate contacts, a plurality of source contacts coupled in parallel and a plurality of drain contacts coupled in parallel; and~~

a plurality of field effect transistors formed using the monolithic semiconductive substrate and comprising a plurality of electrical contacts including a plurality of gate contacts and a plurality of power contacts including source contacts and drain contacts, wherein the field effect transistors are coupled in parallel with one another to form a power

semiconductor switching device and wherein respective ones of the power contacts of the field effect transistors are coupled in common with one another; and

auxiliary circuitry formed using the monolithic semiconductive substrate and configured to couple with at least one of the electrical contacts of the power field effect transistors.

5. (Amended) The circuitry of claim 1 wherein the gate contacts are coupled in ~~parallel~~ common with one another.

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